claimed invention of claims 1-8. Raad discloses an invented memory assembly for mounting atop a microprocessor with the purpose of increasing the speed of signal transfer between the memory and the microprocessor. As part of the Raad structure, there is provided a frame 109, with internal signal leads 111 upon which a pair of memory devices 103 sit and are electrically connected. The internal signal leads 111 connecting the two memory devices in turn sit on top of electrical vias 201, which are electrically connected to the microprocessor 101. The microprocessor 101 itself has external leads 113. Figure 1 of the instant application, which shows a prior art device as having a lead frame 10 with a frame body that serves as a loader for a single integrated circuit chip 11 and that is formed with a chip for receiving window 12 for placing the integrated circuit chip 11 therein. The lead frame 10 is provided with external connection leads 13, and bonding pads 110 are formed on the integrated circuit 11. The bonding pads 110 are usually wire-bounded to the connection leads for electrical connection therewith.

Given these two distinct disclosures, it is unclear how the combination of Raad and te prior art of Fig. 1 could be combined. Even if combined, applicant respectfully believes the function of the Raad device, namely, to permit mounting of the memory atop the microprocessor and connects to electrical vias, would be destroyed since the external leads of the combination would not be able to interconnect to the electrical vias of the microprocessor. Applicant therefore respectfully submits that one having ordinary skill in the art would not find it obvious to combine these two references, and even if they were combined, the result would not be the claimed invention.

The Examiner rejects claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,130,473 to Mostafazadeh et al. Applicant respectfully points out that the Mostafazadeh et al. reference is directed to a lead frame chip scale package wherein a plurality of integrated circuits are bound to a lead frame connected with wire leads, are encapsulated, and are then cut out from individual integrated circuits. Indeed, Figure 1b of Mostafazadeh discloses a lead frame panel with conductive fingers that establish electrical connections between adjacent integrated circuit chips. However, the conductive fingers on the same column of the lead frame panel of the cited Mostafazadeh et al. patent

are interconnected and are cut off during a singulation stage to form individual integrated circuit packages. There is no teaching in this patent that a semiconductor chip package can include at least two integrated circuit chips that are interconnected via internal connection leads, and external leads connected to at least one of the integrated circuit chips in a manner recited in the present claims.

In sharp contrast, in the claimed invention, the frame body is made of a non-conductive material to prevent undesirable electrical connections among the internal and external connection leads. Yet another distinction between the presently claimed invention and that of the Mostafazadeh et al. patent resides in the use of internal connection leads. In the cited patent, the internal connection leads of the lead frame panel of Figure 1b, which are initially interconnected in columns, serve as external connection leads after cutting to form individual integrated circuit packages. Figure 1b of the Mostafazadah patent does not disclose a semiconductor chip package with multiple integrated circuit chips, but instead discloses a lead frame panel populated with integrated circuit chips. In the present invention, the internal connection leads are generally not connected to each other and are generally distinct from the external connection leads. Based on these noted differences, withdrawl of the ground of rejection is requested.

In rejecting the claims as obvious, the Examiner suggests that the claims may be less than perfectly clear, but does not object or reject to the claims under 35 U.S.C. 112 or any other specific basis or point out any specific language lacking clarity. Inasmuch as the applicant can be his own lexicographer, applicant would point out that while use of terminology such as "windows" and "chip receiving windows" are not used in the cited prior art, they are described in detail in the specification, and accordingly are believed to be sufficiently clear.

Based on the foregoing, applicant respectfully submits that the claims as filed recite patentable subject matter, and applicant requests prompt allowance. If the Examiner has any remaining minor issues, a telephone call to the undersigned would be appreciated.

Respectfully submitted,

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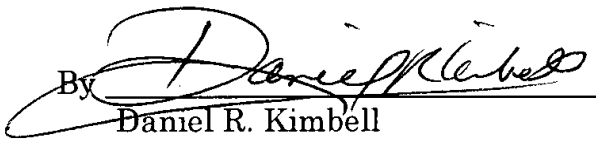
By 

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shows a prior art device as having a lead frame 10 with a frame body that serves as a loader for a single integrated circuit chip 11 and that is formed with a chip for receiving window 12 for placing the integrated circuit chip 11 therein. The lead frame 10 is provided with external connection leads 13, and bonding pads 110 are formed on the integrated circuit 11. The bonding pads 110 are usually wire-bounded to the connection leads for electrical connection therewith.

Given these two distinct disclosures, it is unclear how the combination of Raad and the prior art of Fig. 1 could be combined. Even if combined, applicant respectfully believes the function of the Raad device, namely, to permit mounting of a memory assembly atop the microprocessor, would be destroyed since the external leads of the combination would not be able to interconnect to the electrical vias of the microprocessor. Indeed, given the language of amended claims 1 and 4 of the "unitary frame body", there is no way the cited references could be combined to result in the claimed invention. Applicant therefore respectfully submits that this grounds of rejection is traversed.

The Examiner rejects claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,130,473 to Mostafazadeh et al. The Mostafazadeh et al. reference discloses a fixture and method for providing temporary support to a lead frame during an IC package manufacturing process using a lead frame panel 110 made up of multiple lead frames 120. IC chips are mounted and wire bonded to each lead frame 120 with fine gold wires 140. Each IC chip 130 is encapsulated in a protective casing 160, and then the lead frames 120 are cut apart, or singulated, and multiple electrical interconnections are attached to the lead frame in order to produce individual IC packages 190. See Col. 1, lines 12-26.

Applicant has considered the Mostafazadeh et al. reference, and respectfully believes that the invention as claimed is novel thereover. Applicant believes that there is no teaching or suggestion in the Mostafazadeh et al. reference of the instantly claimed "lead frame for a completed and assembled semiconductor chip package" that includes at least two "chip-receiving windows formed in a unitary frame body" that can include at least two integrated circuit chips that are interconnected via internal connection leads, and external leads connected to at least one of the integrated circuit chips, "to provide an individual semiconductor chip package" in a manner recited in the present amended claims 1 and 4.

Another distinction between the presently claimed invention and that of the Mostafazadeh et al. patent resides in the use of internal connection leads. In the Mostafazadeh et al. patent, the

initially interconnected leads are provided in repeated columns and rows of the lead frame panel 110 (see Figure 1b) and after the manufacturing process is completed, become only external connection leads of individual integrated circuit packages, moreover, not internal leads and external leads. The Mostafazadeh et al. patent does not disclose a semiconductor chip package with multiple integrated circuit chips, but instead discloses a lead frame panel populated with multiple IC chips that will be singulated. In the Mostafazadeh et al. patent, the internal connection leads are all interconnected prior to being cut, and could not serve a unitary frame body for a lead frame for a completed and assembled semiconductor frame body.

Based on the foregoing amendments and remarks, Applicant respectfully solicits prompt allowance. Particularly since this paper is filed after final, if the Examiner has any remaining issues or suggestions, a telephone call to the undersigned would be appreciated.

Respectfully submitted,

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VERSION TO SHOW CHANGES MADE

In the Claims

Please amend claims 1 and 4 as follows:

1. (Amended) A lead frame for a completed and assembled semiconductor chip package, said lead frame comprising:

a unitary frame body;

at least two chip-receiving windows formed in said unitary frame body, each of said chip-receiving windows being adapted to receive a respective integrated circuit chip therein;

a plurality of internal connection leads formed on said unitary frame body adjacent to said chip-receiving windows and adapted to be connected electrically to bonding pads on the integrated circuit chips in said chip-receiving windows such that internal electrical connection among the integrated circuit chips can be established via said internal connection leads; and

a plurality of external connection leads formed on said unitary frame body adjacent to at least one of said chip-receiving windows and adapted to be connected electrically to the bonding pads on the integrated circuit chip in said at least one of said chip-receiving windows, said external connection leads serving as terminal pins such that external electrical connection with the integrated circuit chip in said at least one of said chip-receiving windows can be established via said external connection leads to provide an individual semiconductor chip package.

4. (Amended) A semiconductor chip package comprising:

a lead frame including a unitary frame body and at least two chip-receiving windows formed in said unitary frame body;

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads thereon;

a plurality of internal connection leads formed on said unitary frame body adjacent to said chip-receiving windows, said internal connection leads being connected electrically to said bonding pads on said integrated circuit chips in said chip-receiving windows to establish internal electrical connection among said integrated circuit chips; and

a plurality of external connection leads formed on said unitary frame body adjacent to at least one of said chip-receiving windows, said external connection leads being connected electrically to said bonding pads on said integrated circuit chip in said at least one of said chip-

receiving windows, and serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said chip-receiving windows is established via said external connection leads to provide an individual semiconductor chip package.